AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-4. (Canceled)

5. (Currently amended) A semiconductor memory device comprising:

a semiconductor substrate including a source/drain region and a channel region;

a tunnel oxide film formed on the channel region of the semiconductor substrate and having side walls;

a floating gate formed on the tunnel oxide film and having side walls;

a first insulating film formed on the floating gate and having side walls;

a control gate formed on the first insulating film and having side walls; and

a second insulating film comprising an oxide formed on the control gate, wherein:

the side walls of the tunnel oxide film are at least partially receded from the side walls of the floating gate; and

the second insulating film comprising an oxide covers and contacts each of the side walls of the tunnel oxide film, the side walls of the floating gate, the side walls of the first insulating film and the side walls of the control gate.

6. (Currently amended) A nonvolatile semiconductor memory having a plurality of memory cells formed in a matrix, each memory cell comprising:

a semiconductor substrate including a source/drain region and a channel region;

a tunnel oxide film formed on the channel region of the semiconductor substrate and having side walls;

a floating gate formed on the tunnel oxide film and having side walls;

a first insulating film formed on the floating gate and having side walls;

a control gate formed on the first insulating film and having side walls; and

a second insulating film comprising silicon oxide formed on the control gate, wherein:

the side walls of the tunnel oxide film are at least partially receded from the side walls of the floating gate; and

the second insulating film comprising silicon oxide covers and contacts each of the side walls of the tunnel oxide film, the side walls of the floating gate, the side walls of the first insulating film and the side walls of the control gate.